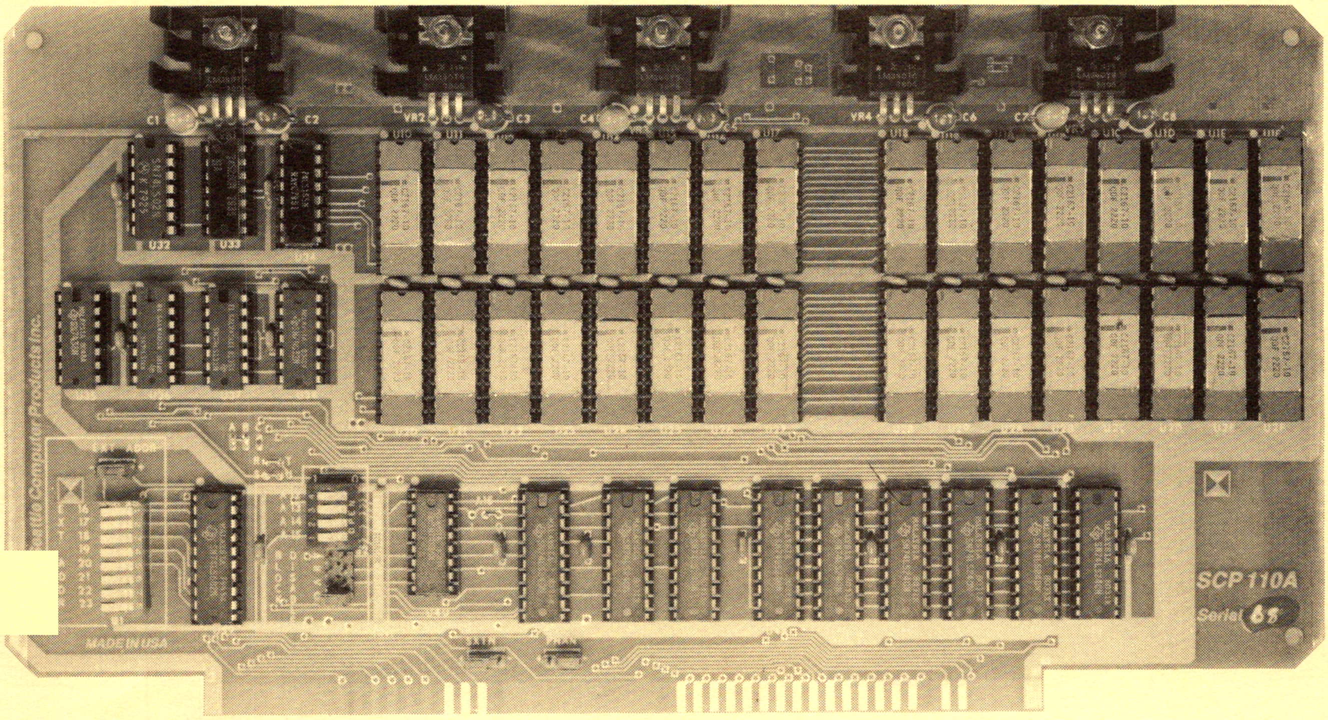
Instruction Manual

Model SCP-110



64K STATIC RAM

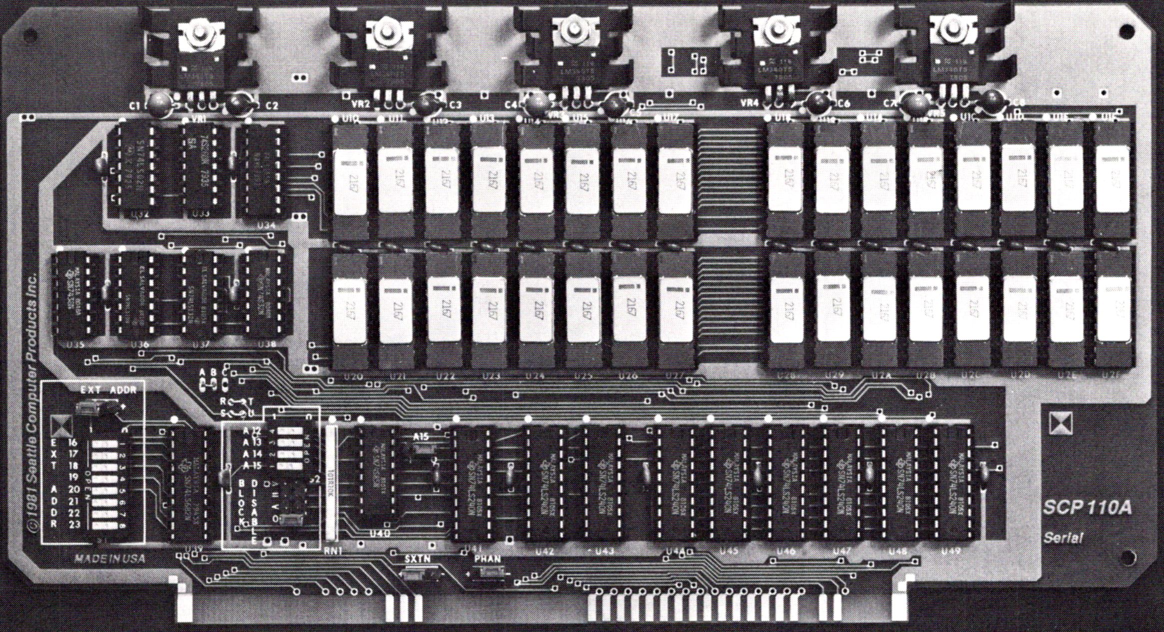
For both 8 and 16-bit S-100 Systems

SEATTLE COMPUTER
1114 Industry Dr. Seattle WA 98188 206/575-1830

Rev. A

64K Static RAM

Model SCP-110



FEATURES

act as either an 8-bit or 16-bit wide
ıory. Dynamic data bus switching per
IEEE Standard.

- Fully static design eliminates system timing problems. Promotes reliable operation with a wider range of CPU cards and DMA devices.
- High Speed - uses new technology 2167 type 100 nsec. chips. Fast enough to allow memory management without wait states.
- Low Power - 64K board typically uses less than 2.5 amps. when active, less when powered-down.
- Can be set to ignore address lines A16-A23 for non-extended address (64K) systems.
- Block disabling feature allows disabling any 4K block, all of the board above a 4K boundary, or all of the board below a 4K boundary.
- Low noise design - all signal inputs to board go through Schmitt trigger buffers.
- Available to OEMs in 16K increments.

SPECIFICATIONS

IEEE S-100 Standard - Fully compatible in all functional specifications.

Memory capacity - 64K bytes. Available in 16K, 32K and 48K variations for OEMs only. 16K and 48K versions are 8-bit wide only.

Memory organization - 64K by 8 bits or 32K by 16 bits. Dynamically switched by state of "Sixteen request" signal. See above for special OEM variations.

Addressing scheme - Extended 24-bit addressing. Upper 8-bits may be disabled. Can be addressed on 64K boundaries over 16-megabyte range.

Memory chip type - fully static 2167 16K by 1 with power-down. 100 nsec. standard; 70 nsec. available at extra charge.

Memory access time from address - 190 nsec. with 100 nsec. chips; 160 nsec. with 70 nsec. chips.

MWRITE pulse width - 45 nsec. minimum.

Data setup prior to end of MWRITE - 47 nsec. minimum.

Data hold after end of MWRITE - 12 nsec. minimum.

Address setup prior to beginning of MWRITE - 71 nsec. minimum.

Address hold after end of MWRITE - 17 nsec. minimum.

Power requirements - 8 volts, 1.5-2.5 amps typical at 25 degrees C, depending on chip manufacturer. 70 nsec. chips typically 2.5 to 3 amps.

Noise margins - all signal inputs to board have minimum of 0.4 volt hysteresis at 25 degrees C.

Operating environment - 5 to 65 degrees C.

Reliability - as this is a new product, no field reliability data is available. Similar SCP products have first year field failure rates of between one and two percent.

WARRANTY AND REPAIR

All SCP hardware is warranted to be free from defects of parts and labor for one year from the date they are sold to the end user. Warranty service is available at the factory with typically 2-day turn-around. Customer must pay shipping to factory, SCP pays shipping to customer.

Factory repair service is available for those products beyond warranty. Typical repair costs are expected to be in the $20 to $50 range, depending upon whether a memory chip replacement is required.

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Configuring the Board

CONFIGURATION SUMMARY

EXT ADDR

EXT ADDR to "+": board uses extended addressing lines A16 - A23.
EXT ADDR to "-": board ignores extended address lines A16 - A23.

EXT ADDR switch (S1) selects one of the 256 64K blocks in which the board can appear. The setting of this switch is irrelevant if the EXT ADDR jumper is set to "-".

A15 JUMPER

This jumper is soldered in place for 64K boards. It is switchable only on 32K versions.

A15 to "0": addresses the board in the lower half of the 64K block.
A15 to "1": addresses the board in the upper half of the 64K block.

BLOCK-DISABLE

ne BLOCK-DISABLE address switch (S2) selects which of the 16 4K blocks (within the 64K block selected by the EXT ADDR switch) will activate the block-disable circuitry.

The BLOCK-DISABLE jumper selects whether:

- < all memory below (less-than) the 4K block selected is disabled
- = the 4K block selected is disabled
- > all memory above (greater-than) the 4K block selected is disabled
- 0 nothing is disabled. In this case, the setting of the BLOCK-DISABLE address switch is irrelevant.

SXTN JUMPER

SXTN to "+": the board responds to sXRTQ* and does sixteen-bit transfers when requested.
SXTN to "-": the board ignores sXTRQ* and always does eight-bit transfers.

PHAN JUMPER

PHAN to "+": the board is disabled when PHANTOM* is active.
PHAN to "-": the board ignores PHANTOM*

CONFIGURATION DETAILS

There are four configuration options which must be set before the board is used:

- Address
- Block-disable
- Sixteen-bit operation
- PHANTOM

ADDRESS

If the system in which this board is to be installed does not have extended addressing (meaning the address space is limited to 64K bytes), then the EXT ADDR jumper should be set to "-". In this way, the board will always respond to a memory access regardless of the state of the extended address lines, A16 - A23.

If the system in which this board is to be installed does uses extended addressing, then this board can be set to any 64K boundary within a 16 Megabyte address space. This is accomplished by setting the EXT ADDR jumper to "+", and setting the desired address on the EXT ADDR switch S1. Printed on the board to the left of the switch are the numbers 16 through 23 which refer to the address lines A16 - A23. Printed on the board above the switch are the two numbers "0" and "1" which refer to the desired level on the address line when the board is to be selected.

> The example shown below in the drawing shows a board addressed at 010000 hex through 01FFFF hex. In this configuration the board will respond when A16 is high and A17 - A23 are low.

```
        1    0
      +--------+
  16  |   <-   |
  17  |   ->   |
  18  |   ->   |
  19  |   ->   |      Extended Addressing Switch - S1
  20  |   ->   |      -------------------------------
  21  |   ->   |
  22  |   ->   |
  23  |   ->   |
      +--------+
```

Processors such as the 8086, which provide twenty significant address lines, usually drive A20 - A23 low. The switch positions corresponding to A20 - A23 should be set to the "0" position for these processors.

A15 JUMPER

If you have a 32K version of this board (jumper B-C installed rather than A-B), then the A15 jumper selects whether the board appears in the top or bottom half of the 64K defined by the EXT ADDR switch. A15 to "0" selects the bottom half, A15 to "1" selects the top half. This jumper is soldered to the "0" position for 64K boards.

BLOCK-DISABLE

This board provides a means by which 4K blocks of memory may be disabled to create "holes" for ROMs, memory-mapped disk controllers, video boards, etc. The block disable works by selecting any 4K block (within the 64K block selected by the EXT ADDR switch) and either disabling that 4K block, disabling all memory locations below that 4K block, or disabling all memory locations above that 4K block. Note: the dividing line between enabled and disabled is the entire 4K block and not the lower boundary of the block.

The address lines A12 - A15 select one of sixteen 4K blocks within the 64K block selected by the EXT ADDR switch. Printed on the board to the left of S2 are the labels A12 - A15 which indicate the address line corresponding to each switch position. Above S2 are the numbers "0" and "1" which select whether the address line in question should be low or high (respectively) when the block-disable circuitry is activated.

If you have a 32K version of the board (jumper B-C installed rather than A-B), it is important to realize that the address selected by S2 is relative to the beginning of the 64K block selected by the EXT ADDR switch rather than from the beginning of the board as selected by the A15 jumper. In other words, if you are using the block-disable features on a 32K board, set the A15 position of S2 to match the setting of the A15 jumper.

Just below S2 is a 2x4 block of pins with a shunt to fit over two of the pins. Printed to the left of the block of pins is a legend explaining the function of each pair of pins. To disable the 4K block selected by S2, put the shunt on the pair of pins to the right of the "=". To disable everything above the selected 4K block, put the shunt on the pins to the right of the ">". To disable everything below the selected 4K block, put the shunt on the pins to the right of the "<". The idea behind using the "<", "=", and ">" symbols is that you can set the board to disable below (less-than), at (equal-to), or above (greater-than) the 4K block selected. We hope this is obvious and that you can set up the board without having to refer to the manual once you become familiar with it. Of course, if none of the board is to be disabled, put the shunt on the pair of pins to the right of the "0". In this position the setting of S2 is irrelevant: the entire board is enabled.

> Example: creating a hole from E000 hex to EFFF hex for a memory-mapped disk controller. Set the address as follows, A12 = 0, A13 = 1, A14 = 1, A15 = 1 (i.e. A12 - A15 = E hex). Put the shunt on the pair of pins to the right of the "=".

```
       1     0
     +---------+
A12  |   ->    |
A13  |   <-    |
A14  |   <-    |
A15  |   <-    |
     +---------+

   <    * *
   =   [* *]
   >    * *
   0    * *
```

Example: 48K memory board which resides between 0 and BFFF hex. In this example we wish to disable everything above the 4K block at B000 hex. Set the address to B hex as follows, A12 = 1, A13 = 1, A14 = 0, A15 = 1. Put the shunt on the pair of pins to the right of the ">".

```
        1     0
      +---------+
A12   |   <-    |
A13   |   <-    |
A14   |   ->    |
A15   |   <-    |
      +---------+

    <   **
    =   **
    >  [**]
    0   **
```

SIXTEEN-BIT OPERATION

If the system in which this board is to be installed does sixteen-bit transfers according to the IEEE-696 standard, the SXTN jumper should be set to the "+" (plus) position. This enables the board to recognize the sXTRQ* signal (bus pin 58) and transfer sixteen bits at a time if requested to do so by the CPU.

If the board is to be installed in an eight-bit system or a system which uses bus pins 58 or 60 for something other than sixteen-bit handshaking, then the SXTN jumper should be set to "-" (minus). This disconnects the board from the sXTRQ* line (bus pin 58) and forces the board to do only eight-bit transfers. In this configuration the SIXTN* driver is effectively disconnected from bus pin 60 since it is never drives that pin.

If you have an eight-bit version of this board (jumpers R-S and T-U installed), then the SXTN jumper should be soldered in place and not switchable. If the SXTN jumper has been installed, it should be set to "-" (minus) because with jumpers R-S and T-U installed, the board is incapable of doing sixteen-bit transfers.

PHANTOM

Some systems use the PHANTOM* line (bus pin 67) to disable memory when a ROM is located at the same address. If you desire this board to be "turned off" by PHANTOM*, set the PHAN jumper to "+", if not, set PHAN to "-".

Theory of Operation

This board is fully compatible with the IEEE-696 standard for S-100 bus interface devices as the standard existed on April 21, 1981. The following theory of operation will not attempt to explain the operation of the S-100 bus and assumes the reader is familiar with the IEEE-696 document.

BOARD-SELECT CIRCUITRY

There are actually two signals generated to indicate whether or not the board is addressed. One is available at U33 pin 5 and is used by the chip-select decoder, U34, to enable chip-selects to the memory when the board is addressed. The status lines are not used in this board-select so sometimes memory chip-selects will be generated during interrupt acknowledge, input, and output cycles. Since the CPU generally spends very little of its time doing these types of bus cycles this shouldn't increase power dissipation significantly. Not using status information to generate chip-selects improves the board access time because the board does not have to wait for status before the chip select process begins.

he other board-select is available at U33 pin 6. This board-select does look at the status lines so is activated only when a memory cycle to the board is occuring. It is used to enable the data utput drivers and the SIXTN* (sixteen-bit acknowledge, bus pin 60) drivers.

The circuitry which decides whether or not the board is addressed is primarily contained in U39 which is a 74LS682 eight-bit magnitude comparator. The "P" inputs which are connected to the eight extended address lines A16 - A23 have low noise hysteresis inputs. The "Q" inputs which are connected to the switch S1 have internal pull-up resistors. The "P=Q" output on pin 19 goes low when the address on the extended-address lines equals the address set on S1.

If the board is a 48K or 64K version, then jumper A-B is installed and A15 does not directly take part in determining if the board is selected. If the board is a 16K or 32K version then jumper B-C is installed and whether or not the board is selected depends on the condition of A15. The A15 jumper selects whether the board is selected when A15 is 0 or 1.

The PHANTOM* signal from the S-100 bus is taken into account when generating the board-select at U33 pin 6. When PHANTOM* goes active (low), board-select is turned off causing the data output drivers and the SIXTN* driver to also be turned off.

CHIP-SELECT CIRCUITRY

The four chip-select lines are generated by U34 which is a 74LS155 decoder. The table below shows how the four chip-select lines are generated in both the eight-bit and sixteen-bit modes. In each ase it is assumed that the board-select from U33 pin 5 is active so that the "B" input to U34 (pin 3) high and PHANTOM* is inactive so that so that the "G" inputs to U34 (pins 2 and 14) are low. If ther of these conditions are not met all chip-select outputs will be inactive (high).

Chip-selects in sixteen-bit mode (jumper R-T and S-U installed) as a function of A15, A0, and sXTRQ*

A15	A0	sXTRQ*	CS0EVEN* (U10-U17)	CS0ODD* (U18-U1F)	CS1EVEN* (U20-U27)	CS0ODD* (U28-U2F)
0	0	1	0	1	1	1
0	0	0	0	0	1	1
0	1	1	1	0	1	1
0	1	0	0	0	1	1
1	0	1	1	1	0	1
1	0	0	1	1	0	0
1	1	1	1	1	1	0
1	1	0	1	1	0	0

Chip-selects in eight-bit mode (jumper R-S and T-U installed) as a function of A15 and A14

A15	A14	CS0EVEN* (U10-U17)	CS0ODD* (U18-U1F)	CS1EVEN* (U20-U27)	CS1ODD* (U28-U2F)
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

In the eight-bit mode (jumper R-S and T-U installed), the SXTN jumper should be soldered in the "-" position so that the 10k pull-up resistor on U41 pin 4 will pull that line high just as if the CPU were always requesting an eight-bit transfer.

BLOCK-DISABLE CIRCUITRY

The block-disable circuitry consists of U40 which is a 74S85 four-bit magnitude comparator and S2 which is the block-disable address switch. U40 compares A12 - A15 on its "A" inputs to the address set on S2 on its "B" inputs. One of the outputs "A<B" (pin 7), "A=B" (pin 6), or "A>B" (pin 5) is selected by the block disable jumper to send to the board-select circuitry. Since the "A" inputs are inverted versions of A12 - A15, the "B" inputs as selected by S2 must be the opposite of the desired level on the address lines A12 - A15. In other words, a closed switch selects a "one" not a "zero" on the address inputs. This also means the "A<B" and "A>B" outputs have reversed meanings, "A<B" goes active (low) when the address on A12 - A15 is greater than the address set on S2 and "A>B" goes active (low) when the address on A12 - A15 is less than the address set on S2.

MEMORY ARRAY

The memory chip used on this board is the 2167-type 16K by 1-bit static RAM. If the board is set up to operate in sixteen-bit mode (jumper R-T and S-U installed), the memory is arranged as two 16K blocks of sixteen-bit words with one 2167 handling each bit. U10 - U1F form the first block and U20 - U2F form the second. Each sixteen-bit word of memory can be accessed as two bytes. In fact, it is usual to think of a sixteen-bit transfer as transfering a pair of bytes, one from an even address, one from an odd address, rather than thinking of an eight-bit transfer as transfering half a word.

U10 - U17 and U20 - U27 form the even bytes, U18 - U1F and U28 - U2F form the odd bytes. This does not mean that the even bytes must be the least-significant bytes and the odd bytes the most-significant, that depends on the CPU. Some CPUs such as the 8086 store the least-significant byte first (in the even location), others such as the Z8000 store the most-significant byte first (in the even location). SCP simply chose to label the even bytes as 0 - 7 and the odd bytes as 8 - F because we manufacture an 8086 CPU and it was convenient for us.

If the board is set up to operate in eight-bit mode (jumper R-S and T-U installed) the memory is arranged as four 16K blocks of bytes. U10 - U17 form the first block, U18 - U1F form the second, U20 - U27 form the third, and U28 - U2F form the fourth.

DATA BUFFERS

There are three 74LS240 octal buffers which drive data from the bus to the memory chips during memory-write cycles. U45 drives data from the DO bus to even bank of memory chips. U46 and U47 form a buffer/multiplexer which drives data from either the DO bus or the DI bus to the odd bank of memory chips. The output-enables of U46 and U47 are connected to the signals IN8* and IN16* (respectively) which come from what looks like an RS flip-flop formed by two sections of U37. However, the real function of this circuit is to insure that as IN8* and IN16* change state, whichever one is going low does so one gate delay after the other went high. This insures that U46 and U47 are never on at the same time, even for few nanoseconds. This is important since the outputs of these buffers are tied together and if both were to turn on at the same time, a surge of current would flow which could cause significant noise on the power supply lines.

The signal IN16* which enables U47 is active during sixteen-bit transfers since the data for the odd memory chips is on the DI bus. During eight-bit transfers, IN8* is active because the data is always on the DO bus during eight-bit transfers. In eight-bit versions of this board (jumper R-S and T-U installed) the SXTN jumper will be set to "-". In this case IN8* will always be on (low) and IN16* will always be off (high). U47 may not have been installed as it is not used in this configuration of the board.

The three 74LS240 octal buffers--U44, U48, and U49--drive data from the memory chips to the bus during memory-read cycles. U44 drives data from the even bank of memory chips to the DO bus during sixteen-bit transfers, U48 drives data from the even bank of chips to the DI bus during eight-bit transfers, and U49 drives data from the odd bank of memory chips to the DI bus during both eight and sixteen-bit transfers. The table below shows the three output-enables OUT16*, OUT8EVEN*, and OUTODD* as a function of A0 and sXTRQ*. This table only applies when the board is run in the sixteen-bit mode (jumpers R-T and S-U installed), and SXTN set to "-". If run in the eight-bit mode, OUT16* never goes active, and either OUT8EVEN* or OUTODD* will be on depending on the state of A14. In any case, the three output enables are gated by pDBIN and board-select so that they only turn on if the data from this board is to be read.

Output-enables in the sixteen-bit mode as a function of A0 and sXTRQ*

A0	sXTRQ*	OUT16*	OUT8EVEN*	OUTODD*
0	1	1	0	1
0	0	0	1	0
1	1	1	1	0
1	0	0	1	0

VOLTAGE REGULATION

Regulation of the eight-volt supply from the S-100 bus is provided by five 7805-type voltage regulators. VR1 supplies regulated power to all the TTL circuitry on the board. VR2 - VR5 each provide power to eight memory chips. C1 - C8 are tantalum electrolytic capacitors which keep the regulators from oscillating and provide filtering of relatively low frequency noise. In addition there are 27 .1 uF ceramic capacitors scattered around the board which suppress high frequency noise on the power supply lines.

Trouble-Shooting

This trouble-shooting section is limited to a discription of the memory array so that bad memory chips found by a memory test can be replaced. Faults in the TTL memory support circuitry can produce such widely varying symptoms that it is not practical to provide trouble-shooting information on them. The THEORY OF OPERATION section of this manual provides some information on the operation of the TTL circuitry for readers doing their own repairs.

MEMORY ARRAY ORGANIZATION AND MEMORY CHIP IDENTIFICATION, SIXTEEN-BIT VERSION.

When this board is jumpered for the sixteen-bit mode (jumpers R-T and S-U installed) the memory is organized as two 32K blocks of bytes. Sixteen ICs form each 32K block, U10 - U1F form the first and U20 - U2F form the second. Within each block the even and odd bytes are interleaved so that eight memory chips (one for each bit) are accessed on transfers to an even address and another eight are accessed on transfers to an odd address. Sixteen-bit transfers access all sixteen memory chips in a block simultaneously to read or write sixteen-bits. The "ones" digit of the memory chip's IC number indicates which bit it handles, 0 - F. This bit number scheme is only valid if the memory is accessed sixteen bits at a time by a CPU such as an 8086 which stores the least-significant byte of a sixteen-bit word first in memory. The ICs representing bits 0 - 7 are really bits 0 - 7 (respectively) of the even bytes, the ICs representing bits 8 - F are really bits 0 - 7 (respectively) of the odd bytes. The diagram below shows a pictorial representation of the memory array.

Memory array in sixteen-bit mode.

	Even byte								Odd byte								Block address
Bit number	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
IC number (block 1)	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0000 - 7FFF hex
IC number (block 2)	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	8000 - FFFF hex

Example: Assume a memory test indicated that bit 5 in location 97E5 hex (relative to the beginning of the board) is bad. Since this address is above the 32K boundary (at 8000 hex), we know that the bad chip is in the second block, U20 - U2F. The location is at an odd address so the bad chip is one of U28 - U2F. Within that group, bit 5 means U2D is the chip in question.

MEMORY ARRAY ORGANIZATION AND MEMORY CHIP IDENTIFICATION, EIGHT-BIT VERSION.

When this board is jumpered for eight-bit mode (jumpers R-S and T-U installed) the even and odd bytes are not interleaved as in the sixteen-bit mode. Instead, the memory is arranged as four 16K blocks of bytes. U10 - U17 are the eight bits of the first block, U18 - U1F are the second block, U20 - U27 are the third, and U28 - U2F are the fourth.

Memory array in eight-bit mode.

Bit number	0	1	2	3	4	5	6	7	Block address
IC number (block 1)	10	11	12	13	14	15	16	17	0000 - 3FFF hex
IC number (block 2)	18	19	1A	1B	1C	1D	1E	1F	4000 - 7FFF hex
IC number (block 3)	20	21	22	23	24	25	26	27	8000 - BFFF hex
IC number (block 4)	28	29	2A	2B	2C	2D	2E	2F	C000 - FFFF hex

Example: Assume the memory test gives the same address, 97E5 hex, and same bit, bit 5, as in the example for the sixteen-bit mode above. In this case we see that 97E5 hex is between 8000 hex and BFFF hex so the bad chip is one of U20 - U27. Since bit 5 is bad we know that the bad chip is U25.

Repair Service

Repair service is available at the factory for any product manufactured by Seattle Computer Products. For items under warranty, there is no charge for this service. For repair of this board when it is no longer under warranty, return the board to the factory address shown below. It is expected that repair costs for this board will be in the $20 to $50 range, depending upon whether a memory chip replacement is required. Normal factory repair time is 48 to 72 hours. Ship all returned boards to:

Seattle Computer Products

1114 Industry Drive

Seattle, Washington 98188

Specifications

Meets all electrical and timing specifications for the IEEE-696 S-100 bus standard.

Memory capacity - 64K bytes. Available in 16K, 32K, and 48K versions to OEMs only. 16K and 48K versions are eight-bit only.

Memory organization - 64K by eight bits. Sixteen bit transfers access two bytes simultaneously as specified by the IEEE-696 standard. See above for special OEM variations.

Addressing scheme - extended twenty-four-bit addressing. Can be set to ignore upper eight address lines in systems with 64K address space. Can be addressed on 64K boundaries in sixteen-megabyte extended address space. 32K versions can be addressed on 32K boundary.

Memory chip type - fully static 2167-type 16K by 1 bit with power-down. 100 nanosecond chips standard, faster chips available at extra cost.

Timing specifications:

> Memory access time (address valid to data valid) - 190 nS with 100 nS chips. Access time for other chips is chip access time from chip-select plus 90 nS.
>
> Memory access time from pDBIN high (assuming address setup time has been met) - 59 nS maximum.
>
> MWRITE pulse width - 45 nS minimun.
>
> Data setup prior to trailing edge of MWRITE - 47 nS minimum.
>
> Data hold after trailing edge of MWRITE - 12 nS minimum.
>
> Address setup prior to leading edge of MWRITE - 71 nS minimum.
>
> Address hold after trailing edge of MWRITE - 17 nS minimum.

Power requirements - 8 volts @ 1.5 to 2.5 amps typical when board is addressed during a sixteen-bit transfer at 25 degrees C depending on chip manufacturer. When board is not addressed chips are in power-down mode and board takes .8 to 1.2 amps typically.

Input hysteresis - all input have 0.4 volt minimum hysteresis at 25 degrees C to improve noise margins.

Operating environment - 5 to 65 degrees C.

Reliability - as this is a new product, no field reliability data is available. Similar SCP products have first year failure rates of between one and two percent.

Special Instructions for 48K version of SCP 64K RAM

The 48K version of this board is intended to replace bank-selected memory in multi-user operating systems such as Digital Research's MP/M. Systems such as this typically have about 16K of memory that is always resident in the system and used for the operating system and several bank selected-boards of about 48K each for different users and tasks. This board uses extended addressing rather than bank select. To use this board with bank-select software, there must be an eight bit latch driving the extended address lines. This latch would be programmable by the CPU. Many newer Z80 CPUs have this feature. If yours does not, there are S-100 cards available which consist of a port decoder and latch which will do the job nicely.

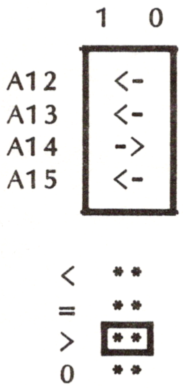
The eight-bit number on the extended address lines is simply a bank number from 0 to 255. Set the extended address switch on the 48K board to match the desired bank number. Note that with this bank select scheme it is not possible to have more than one bank on at a time.

The 48K version is nothing more than a 64K board with eight memory chips removed. For use with MP/M, U28 - U2F (the top 16K) are removed. It is also possible to remove the bottom 16K consisting of U10 - U17 rather than the the top 16K. In order to keep the board from responding to memory reads in the area where the chips have been removed, it is necessary to use the board's block-disable feature.

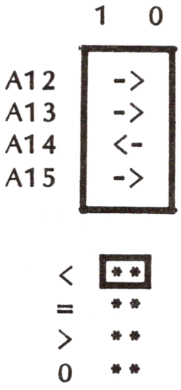
If the top 16K is removed, set the block-disable address to "B" and the block-disable jumper to ">". This will disable all memory above the 4K block at B000 hex which is C000 - FFFF hex. If the operating system requires more than 16K, more of the 4K blocks can be disabled by moving the block disable address down 4K at a time to "A" or "9".

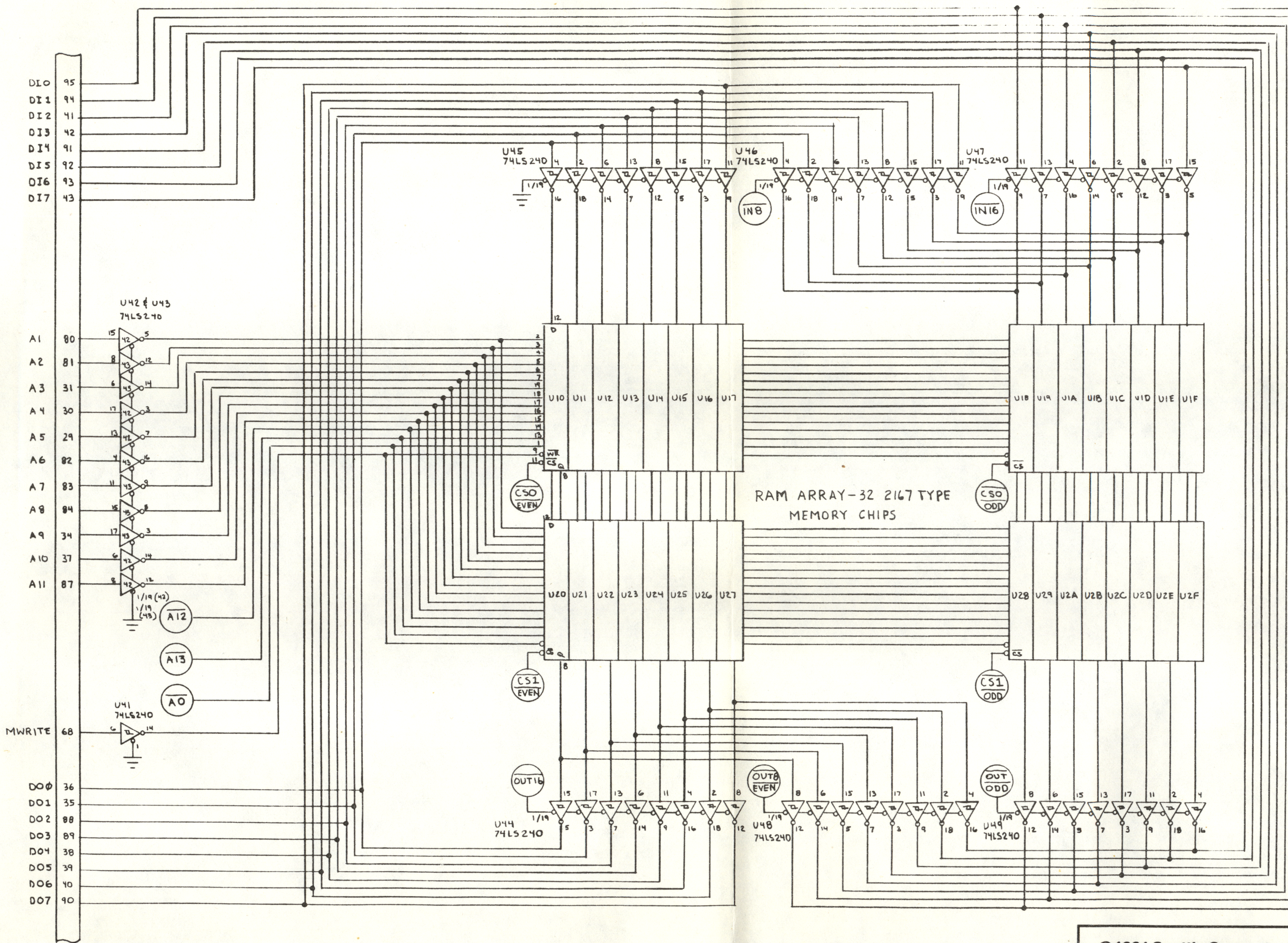
If the bottom 16K is removed, set the block-disable address to "4" and the block-disable jumper to "<". This will disable all memory below 4000 hex which is 0000 - 3FFF hex. If more than 16K is to be disabled, the block-disable address can be moved up 4K at a time.

48K from 0 - BFFF hex



48K from 4000 - FFFF hex





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64K STATIC RAM CARD		
SCHEMATIC	SH 1 OF 2	DRAWING NUMBER SCP-110A

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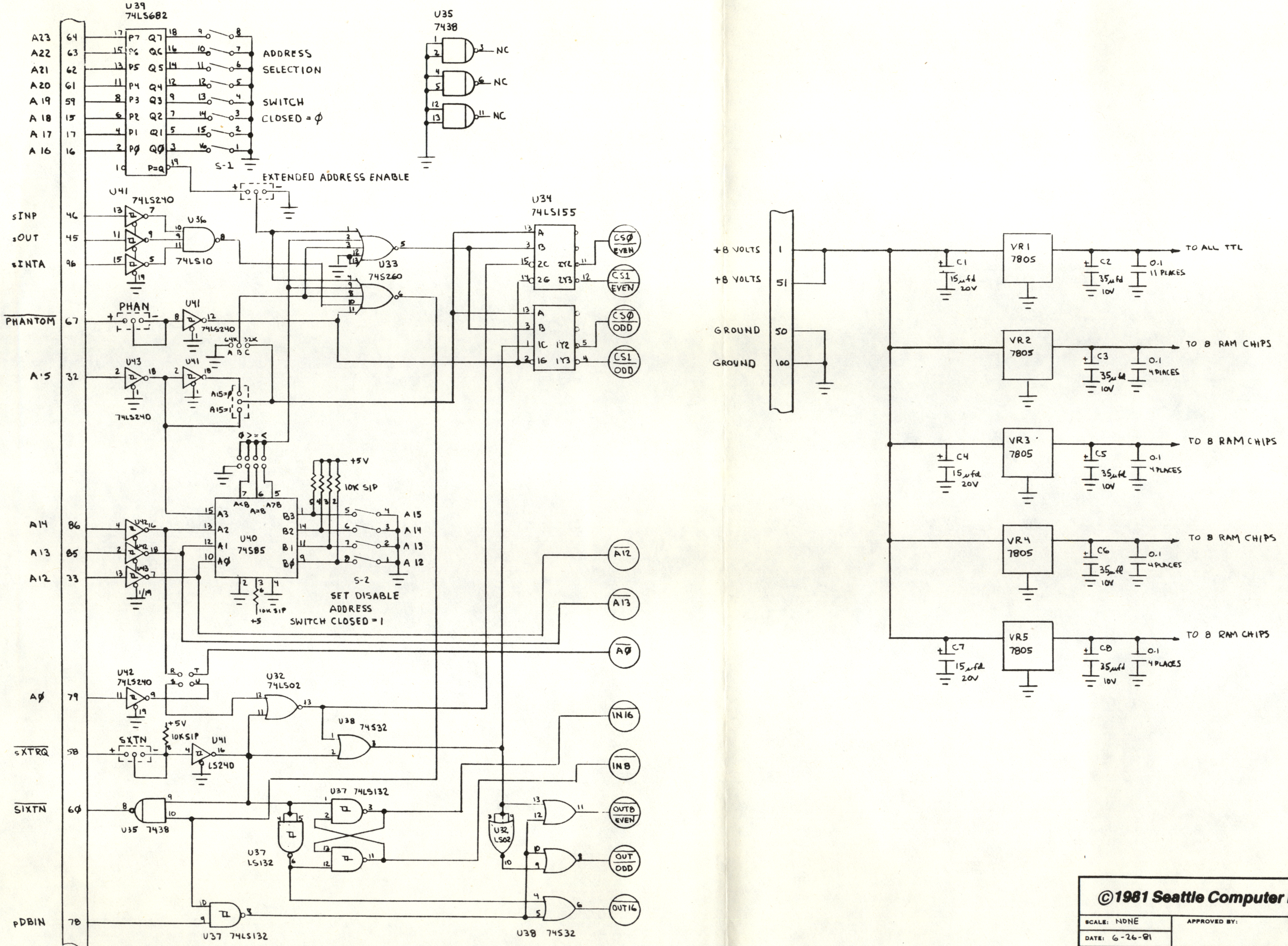

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